Application Note 355
Test Registers

Note:

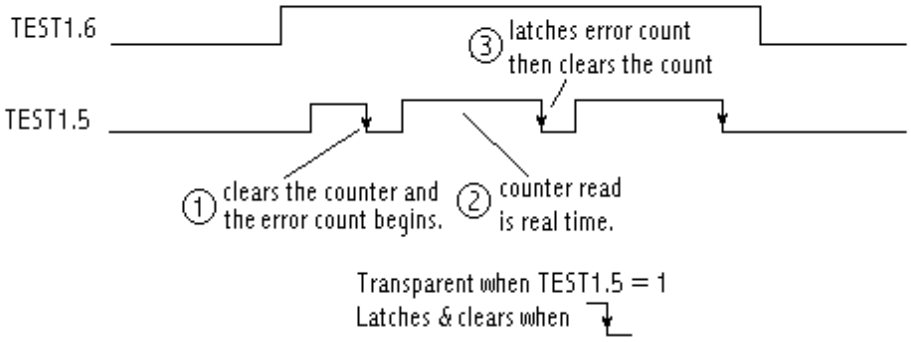
For DS21Q42 and DS21Q44 devices, the Line Interface TEST registers are not applicable.

Test Register Settings for the DS21x52 & DS21Q42

1. **TEST1 (address 7D)** can be used for error counter functionality.

TEST1.6	Set High to Enable Test1.5 to control sampling of error counters
TEST1.5	Sample error counters. (See figure below)

Point 1: After TEST1.6 is set high, toggling TEST1.5 clears the counter and starts the error counter.
Point 2: The actual count is transparent to the user while TEST1.5 is set high. The user will then see the accumulated error count from the time of reset to setting TEST1.5 high.
Point 3: When TEST1.5 is cleared, the error count is latched and the count is reset and allowed to begin counting.



TEST1.3 resets the one second timer.

1. **TEST2 (address 09)** can be used to modify the Attenuation Levels of the device

TEST2.7	TEST2.6	TEST2.5	TEST2.4	TEST2.1	OUTPUT
0	1	1	0	X	Rcvr additional 6dB attenuation pad
0	1	1	1	0	Rcvr 20dB monitor mode
0	1	1	1	1	Rcvr 12dB monitor mode
1	0	0	0	1	Bypass equalizer

1. Common Control bits settings (address 0A)

CCR7.2 = 1	Line Interface Synchronization Interface Enable
CCR7.1 = 1	Customer will generate a CDI pattern at TTIP & TRING instead of normal data.
CCR7.0 = 1	TTIP & TRING become open drain

Test Register Settings for the DS21x54 & DS21Q44

1. **TEST1 (address 15)** can be used for output test mode and error counter functionality.

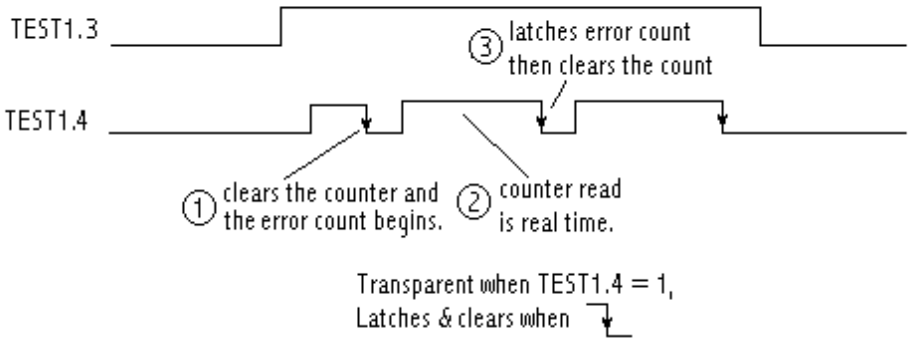
   TEST1.7 and TEST1.6 can be used to force all outputs into a logic 1, logic 0 or 3-state.

TEST1.7	TEST1.6	OUTPUTS
0	0	NORMAL OPERATION
0	1	3-STATE
1	0	LOGIC '0'
1	1	LOGIC '1'

   TEST1.4 and TEST1.3 can be used for error counter functionality.

TEST1.4	Sample error counters. (See figure below)
TEST1.3	Set High to Enable Test1.4 to control sampling of error counters

Point 1: After TEST1.3 is set high, toggling TEST1.4 clears the counter and starts the error counter.
Point 2: The actual count is transparent to the user while TEST1.4 is set high. The user will then see the accumulated error count from the time of reset to setting TEST1.4 high.
Point 3: When TEST1.4 is cleared, the error count is latched and the count is cleared.



   TEST1.2 =1 converts SR2.0 from TSLIP to Loss of Receive Clock (LORC).
   TEST1.0 resets the one second timer.

2. **TEST3 (address AC)** can be used to modify the Attenuation Levels of the device

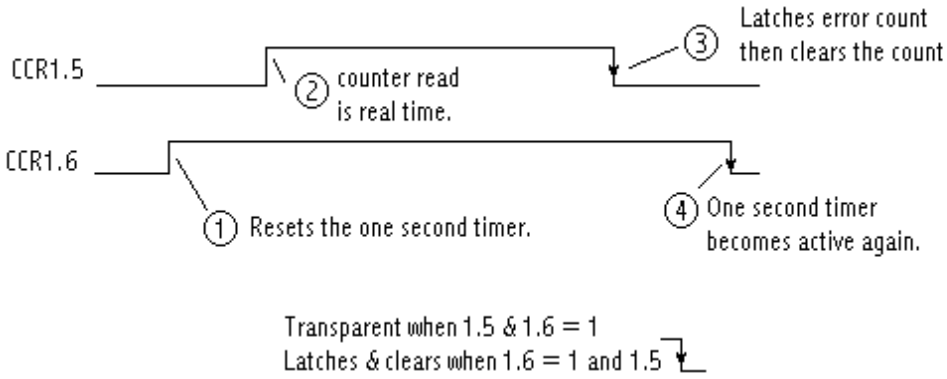
TEST3.7	TEST3.6	TEST3.5	TEST3.4	TEST3.1	OUTPUT
0	1	1	0	X	Rcvr additional 6dB attenuation pad
0	1	1	1	0	Rcvr 30dB monitor mode
0	1	1	1	1	Rcvr 12dB monitor mode
1	0	0	0	1	Bypass equalizer

Test Register Settings for the DS2152

1. **CCR6 (address 1E)** can be used for error counter functionality.

CCR1.6	reset one second timer
CCR1.5	testcount. (See figure below)

Point 1: Setting bit 6 high prohibits the 1 second timer from interfering with the error count.
Point 2: While bit 6 is high, asserting bit 5 allows the counter to begin. The counter read is real time.



2. **TEST2 (Address 09)** can be used to modify the Attenuation Levels of the device.

TEST2.6	TEST2.1	TEST2.0	OUTPUT
1	0	0	Rcvr additional 6dB attenuation pad
0	1	0	Rcvr 6dB monitor mode
0	0	1	Bypass equalizer

Test Register Settings for the DS2154

1. TEST2 (address19)

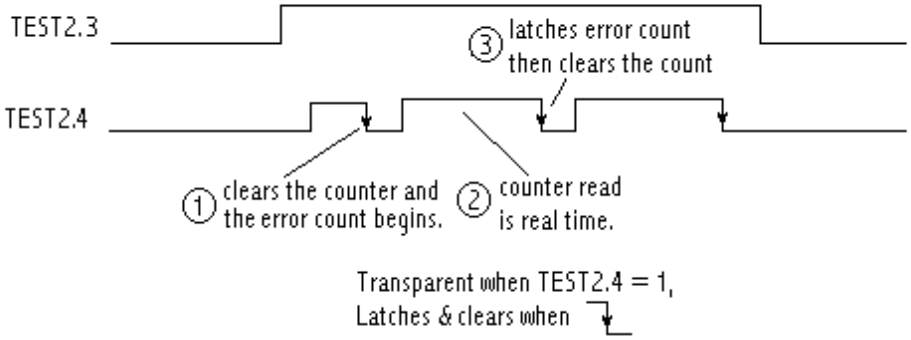
OUTPUT TEST MODES TEST2.7 and TEST2.6 can be used to force all outputs into a logic 1, logic 0 or 3-state.

TEST2.7	TEST2.6	OUTPUTS
0	0	NORMAL OPERATION
0	1	3-STATE
1	0	LOGIC '0'
1	1	LOGIC '1'

TEST2.4 and TEST2.3 can be used for error counter functionality.

TEST2.4	Sample error counters. (See figure below)
TEST2.3	Set High to Enable Test1.4 to control sampling of error counters

Point 1: After TEST2.3 is set high, toggling TEST2.4 clears the counter and starts the error counter.
Point 2: The actual count is transparent to the user while TEST2.4 is set high. The user will then see the accumulated error count from the time of reset to setting TEST2.4 high.
Point 3: When TEST2.4 is cleared, the error count is latched and the count is cleared.



TEST2.2 will change the definition of RIR.7, RIR.6 and SR2.0.

TEST2.2	RIR.7	RIR.6	SR2.0
0	NORMAL (TESF)	NORMAL (TESE)	NORMAL (TSLIP)
1	RL1, RECEIVE LEVEL BIT 1	RL0, RECEIVE LEVEL BIT 0	LORC, LOSS OF RECEIVE CLOCK

RL1	RL2	TYPICAL LEVEL RECEIVED
0	0	+2dB to –7.5dB
0	1	-7.5dB to –15dB
1	0	-15dB to –22.5dB
1	1	Less than –22.5dB

Setting TEST2.1 = 1 will cause the receive framer to determine if a RCL state exist. Normally (TEST2.1 = 0) the LIU determines the RCL state.

Setting TEST2.0 = 1 will reset the one second timer.

1. **TEST3 (Address AC)** can be used to modify the Attenuation Levels of the device.

TEST3.6	TEST3.1	TEST3.0	OUTPUT
1	0	0	Rcvr additional 6dB attenuation pad
0	1	0	Rcvr 6dB monitor mode
0	0	1	Bypass equalizer